A CASE STUDY IN SIMULATION METHODS FOR POWER ELECTRONIC CIRCUITS

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ABSTRACT

Motivated by the challenge of capturing the new discrete dynamics that fundamentally characterize modern grid technologies, we revisit the problem of simulating power electronic circuits. A simplified circuit is used as a case study to uncover and highlight key considerations in the use of traditional numerical simulation methods and compare them with those obtained from alternative methods that are discrete event-based from the outset. Results show the regimes where the traditional numerical methods and the alternative discrete event methods are applicable, and the need for discrete event approaches that precisely and efficiently resolve switching dynamics produced by power electronics systems that are important in emerging grid scenarios, such as large scale renewable energy.

Keywords: discrete event, numerical method, fixed time step, variable time step

1 INTRODUCTION

Popular circuit simulation packages have historically emphasized the simulation of analog circuits. For tools in the Electro-Magnetic Transient Program (EMTP) family, such as PSCAD and EMTP-RV (Manitoba Hydro International 2018, Mahseredjian, Karaagac, Dennetiére, and Saad 2015), this focus has resulted in a rather sophisticated use of the fixed step trapezoidal method (Dommel 1986). Variable step methods are common in the SPICE family of circuit solvers (Nagel and Pederson 1973). Surprisingly absent from many of these simulators are precise techniques for handling discrete events. The impact of this omission for power electronics simulations are a loss of computational efficiency, the introduction of significant numerical artifacts, or both.

In the context of power system simulations, these deficiencies were of only slight importance for modeling a fundamentally analog system (Ametani 2020). However, a rapidly expanding role for power electronics

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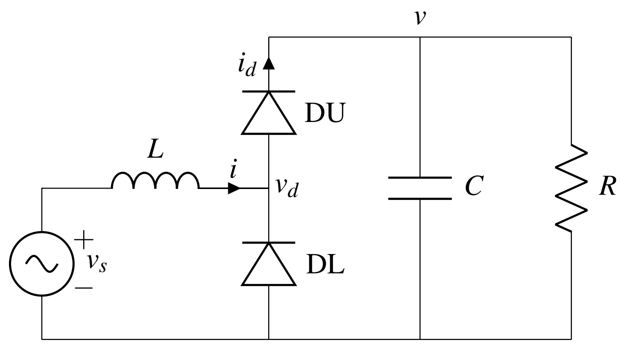

Figure 1: The test circuit

in the smart grid is poorly matched by modeling techniques optimized for analog electrical networks. We offer a brief case study of how the precise inclusion of discrete event dynamics improves the performance of circuit simulations that involve power electronics while avoiding new numerical artifacts caused by introducing discrete modes of operation. Our case study is a simple circuit that poses significant challenges for both fixed step and variable step size numerical integration without precise handling of discrete events.

The issues raised here are related too, but distinct from, numerical oscillation problems inherent in the trapezoidal method; see, e.g., (Zhao, Fan, and Gole 2020, Ferreira, Bonatto, Cogo, de Jesus, Dommel, and Martí 2015). Numerical oscillations in the trapezoidal method are caused by discontinuous changes in continuous state variables, and this problem can be resolved by using a different integration technique; see, e.g., (Gao, Solodovnik, Dougal, Cokkinides, and Meliopoulos 2003, Noda, Takenaka, and Inoue 2009).

The oscillations discussed in this article stem from omitting discrete modes of operation in the model. Hence, the problem can be resolved only if the simulation method permits the inclusion of discrete modes and discrete events for transitioning between them. This is a well known problem in the context of simulation methods for hybrid dynamic systems, but it is often unfamiliar to the users of domain specific modeling tools, such as circuit simulators. We highlight the problem with a simple, but representative, power electronics model. By doing so, we seek to raise awareness of the technical issues that manifest as simulation errors, and to demonstrate the efficacy of established methods for resolving these errors.

2 THE TEST MODEL

The circuit for our case study is show in Fig. 1. This circuit is a simple converter of alternating voltage to direct voltage. The diodes ensure continuity of the line containing the inductance as the current alternates between positive and negative flow. A positive current through the inductance flows through upper diode DU to charge the capacitor. Negative current flows through the lower diode DL. Because current cannot leave the capacitor through DU, the output voltage rises until it reaches a value such that DU can no longer be positively biased by the voltage source. If the resistance is large, the capacitor becomes fully charged, at which time its voltage is essentially constant.

The simplest mathematical model of this circuit uses lumped elements for the capacitance, resistance, and inductance. The dynamics of these elements are described by

$$v_s = A\sin(2\pi f t) \tag{1}$$

$$di/dt = (v_s - v_d)/L \tag{2}$$

$$dv/dt = (i_d - v/R)/C \tag{3}$$

where $A = 480\sqrt{2}$, $f = 60$, $R = 10^{10}$, and $L = C = 0.001$. The initial conditions are $t = i = v = 0$.

The diodes play a primary role in the evolution of i_d and v_d. A diode is modeled by an open switch when the current through it is zero. When a positive current f flows through the diode with a positive voltage u, these are related by

$$u = g(f) = v_T \ln(f/I_s + 1) \tag{4}$$

In our model, $I_s = 10^{-6}$ and $v_T = 0.04$. We omit the small reverse current that occurs when the diode is reverse biased. Hence, the diode requires $f > 0$ if, and only if, $u > 0$. Similarly, $f = 0$ if, and only if, $u \leq 0$. When $f = 0$ there is no restriction on the negative voltage and the element acts like an open circuit.

The diodes introduce three distinct modes of operation for i_d and v_d. The simplest are when $i \neq 0$. In this case, we have

$$i_d = \begin{cases} i & i > 0 \\ 0 & \text{otherwise} \end{cases} \tag{5}$$

$$v_d = \begin{cases} -g(-i) & i < 0 \\ v + g(i) & i > 0 \end{cases} \tag{6}$$

The model's behavior is more complex when $i = 0$. At an instant when $i = 0$ both diodes act as open circuits and so $v_d = v_s$. If $v_d = v_s > v$ and an infinitesimal moment later v_s increases then i becomes positive and the upper diode conducts. On the other hand, if $v_d = v_s = 0$ and an infinitesimal moment later v_s decreases then i becomes negative and the lower diode conducts. If v_s does not leave these bounds then i remains at zero.

This is the correct behavior, which is realized efficiently with an algorithm managing discrete events. Without such an algorithm, a time stepped simulator will almost certainly overshoot $i = 0$. When this happens, the behavior of the model is governed by Eqns. 6 and 5 without consideration of the $i = 0$ condition. As v_d swings between zero and v, i moves a small distance back and forth across zero.

These oscillations of i and v_d are numerical artifacts; they do not appear in correct solutions of the model's equations. In a fixed-step solver, the magnitude of these errors will be proportional to the step size. A variable step solver will use its inbuilt error control scheme to limit – but not eliminate – the error. As we will see, it does so by using a small step size to keep i near zero.

3 COMPARISON OF SOLUTION METHODS

We compare three solution methods, each using corrected Euler to simulate the continuous state variables. The fixed-step solution uses a single step size throughout the simulation execution. The variable step solution adapts the step size to remain within an error tolerance but without the benefits of an algorithm for event handling. The event driven solution uses corrected Euler with an adaptive step size and adds to it a root finding algorithm for event detection (Nutaro 2010, Cellier and Kofman 2006). Each simulation is conducted using the adevs simulation package (Nutaro 2020). Source code for the simulations is available in the examples folder of that package; the file is `diode.cpp`. In each case, we simulate a full period of the input voltage. The results of our comparison are summarized in Table 1.

3.1 Fixed step simulation

With a fixed step size, the quality of the solution depends strongly on the step size selection, which forces the user to trade accuracy for computational time. Moreover, experiments with a simple model may be needed to select an appropriate step size without guarantees that a similar step size would produce acceptable results in another model.

Simulation method	Method parameters	Steps required	Qualitative features
Fixed step	1 ms time step	34	Errors and numerical oscillations in proportion to step size
	100 μs time step	334	
	10 μs time step	3,334	
	1 μs time step	33,334	
Variable step	0.1 error tolerance	46,889	Errors, numerical oscillations, and step choice in proportion to tolerance
	0.01 error tolerance	460,384	
	0.001 error tolerance	4,568,758	
Discrete event	0.1 error tolerance	1,086	Errors and step choice in proportion to error tolerance, eliminating numerical oscillations reduced step count
	0.01 error tolerance	3,245	
	0.001 error tolerance	9,974	

Table 1: Summary of method comparison. Maximum errors are reported in relation to the discrete event solution.

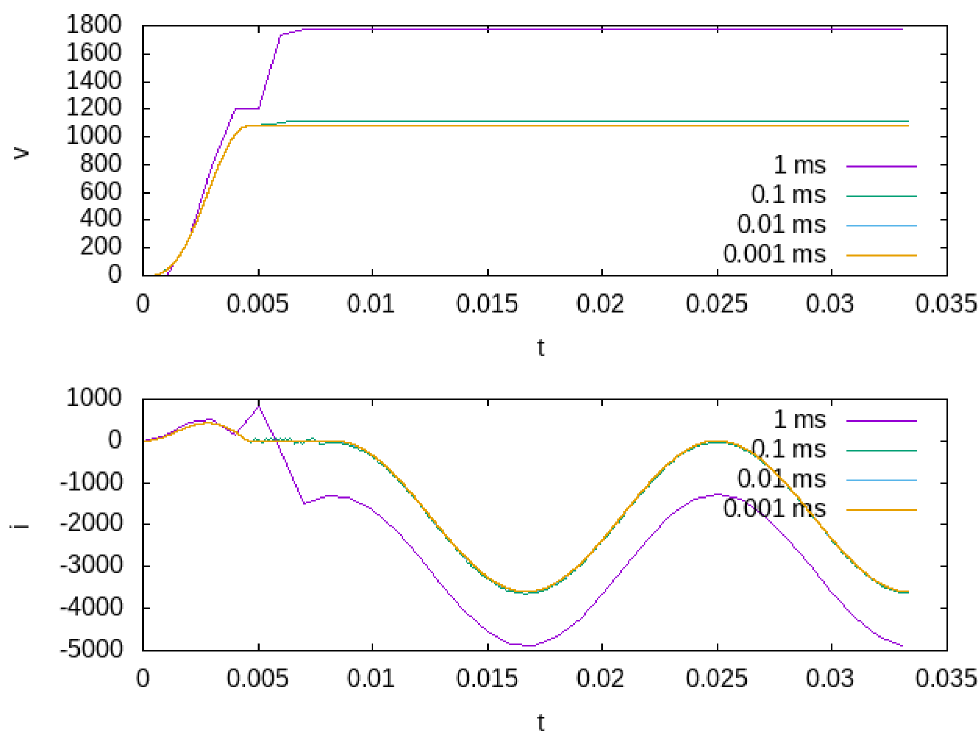

Figure 2: Current and voltage for several step size choices using the fixed step simulation method.

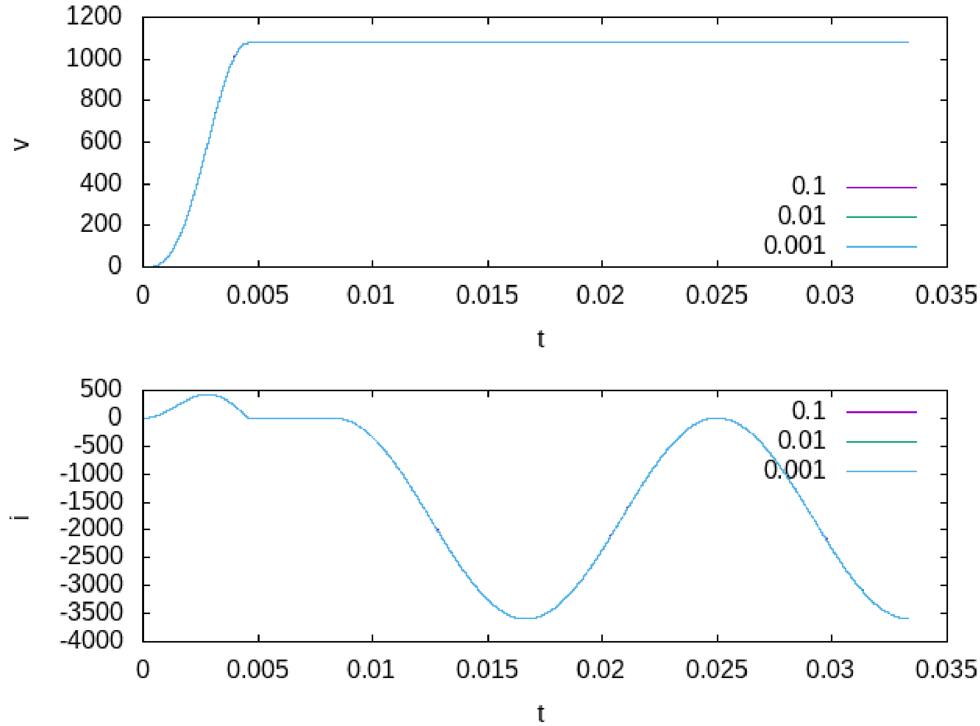

Figure 3: Current and voltage for several error tolerance choices using the variable step simulation method.

Figure 2 shows v and i calculated using several choices of the simulation step size. Oscillations of i are readily apparent and their magnitude grows with the step size. The trajectory of v is similarly sensitive to the step size of the simulation. This sensitivity is not unexpected. The fixed step size method assumes continuity of the model's trajectories, but this assumption is violated by Eqn. 6 which causes discontinuous jumps in v_d. The computational effort is proportional to the step size, ranging from 34 steps for 1 ms to $33,334$ steps for 1 μs.

3.2 Variable step simulation

We fix the maximal step size at 1 ms and change the relative error tolerance of the variable step solver. The effect of the relative tolerance on i and v are shown in Fig. 3, but at this scale the solutions overlap very closely. Automatic error control improves the quality of the solution by keeping i near zero while the capacitor is fully charged and the input voltage is positive. However, this improvement in the solution comes at a considerable computational cost. A simulation with error tolerance 0.1 requires 46,889 steps, an error tolerance of 0.01 needs 460,384 steps, and error tolerance of 0.001 requires 4,568,758 steps!

The oscillations of i near zero are less apparent in Fig. 3. Nonetheless, numerical oscillations are present, affecting both the solution and the computational effort. A closeup of the current in the region of oscillation induced by the simulation method is shown in Fig. 4.

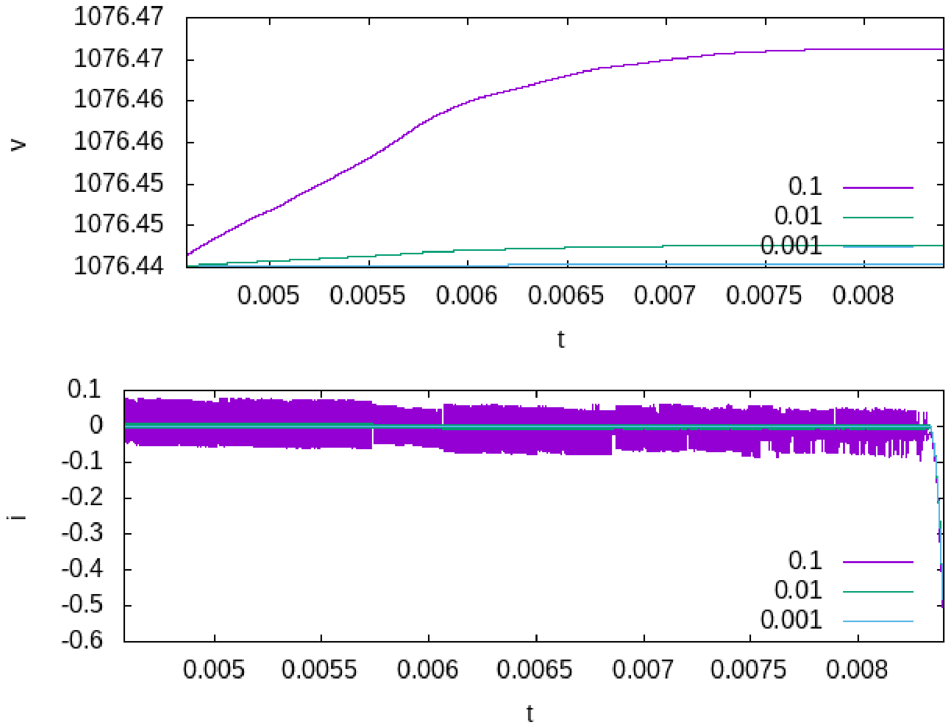

Figure 4: Closeup view of oscillating current in Fig. 3.

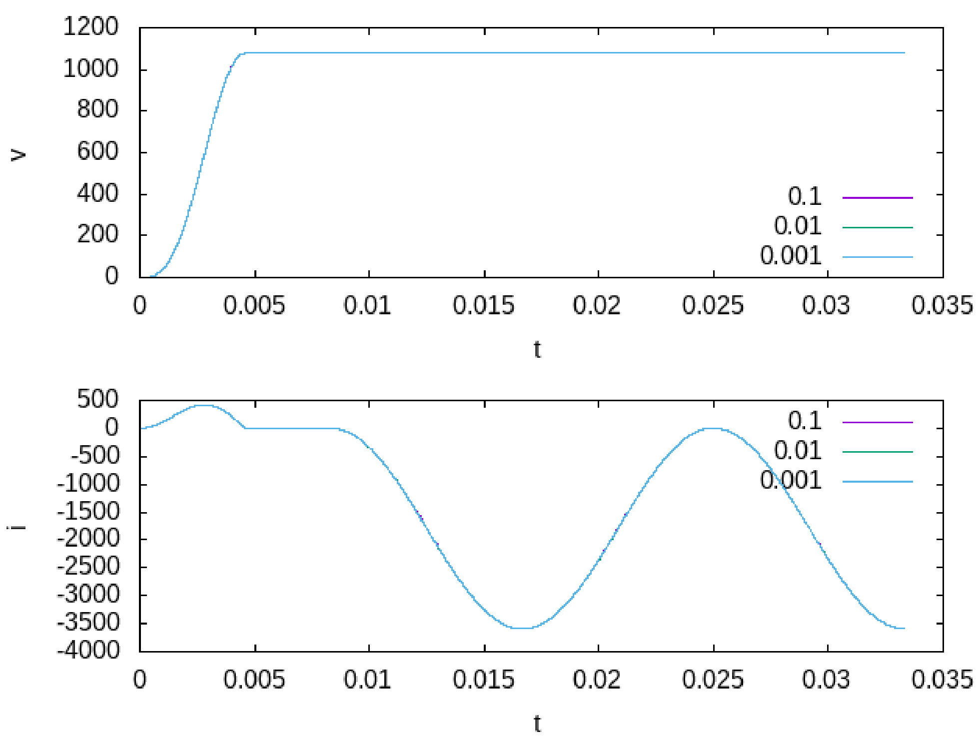

Figure 5: Current and voltage for several error tolerance choices using the discrete event simulation method.

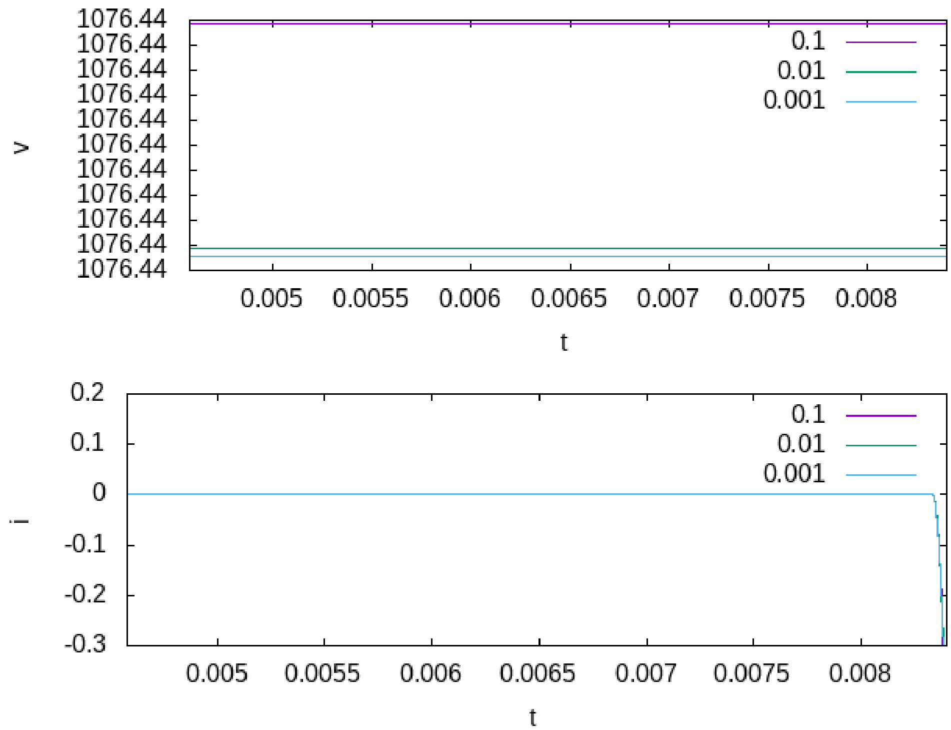

Figure 6: Closeup view of Fig. 5 in the region where fixed and variable step methods induce oscillations.

3.3 Discrete event simulation

As with the variable step size simulation, we compare several choices of the relative error tolerance for the corrected Euler algorithm. However, we also introduce explicit event handling using the method of zero crossing functions described in (Nutaro 2010, Cellier and Kofman 2006). In this version of the model, discrete events cause the model to alternate between three distinct modes of operation: NONE, DU, and DL. Zero crossing functions define transition conditions that depend on the discrete mode and continuous state variables. Mode transitions occur at the instant that the zero crossing occurs.

The mode NONE models $i = 0$ in which neither diode is conducting. This case is not be accounted for by the fixed step and variable step simulations. We leave mode NONE when $v_s = 0$ or $v_s = v$. The zero crossing function is

$$z(v_s, v_c) = v_s(v_s - v) \tag{7}$$

and while in this mode

$$i_d = 0 \tag{8}$$

$$v_d = v_s \tag{9}$$

Upon leaving mode NONE, we may enter mode DU with the upper diode conducting or mode DL with the lower diode conducting. We transition from NONE to DL as v_s becomes negative and from NONE to DU as v_s climbs above v. The mode DU corresponds to the $i > 0$ case in Eqns. 6 and 5, and DL corresponds to the $i < 0$ case.

We transition out of DL as i transitions from negative to positive. Similarly, we transition out of DU as i transitions from positive to negative. In practice, our numerical solutions require a small hysteresis value

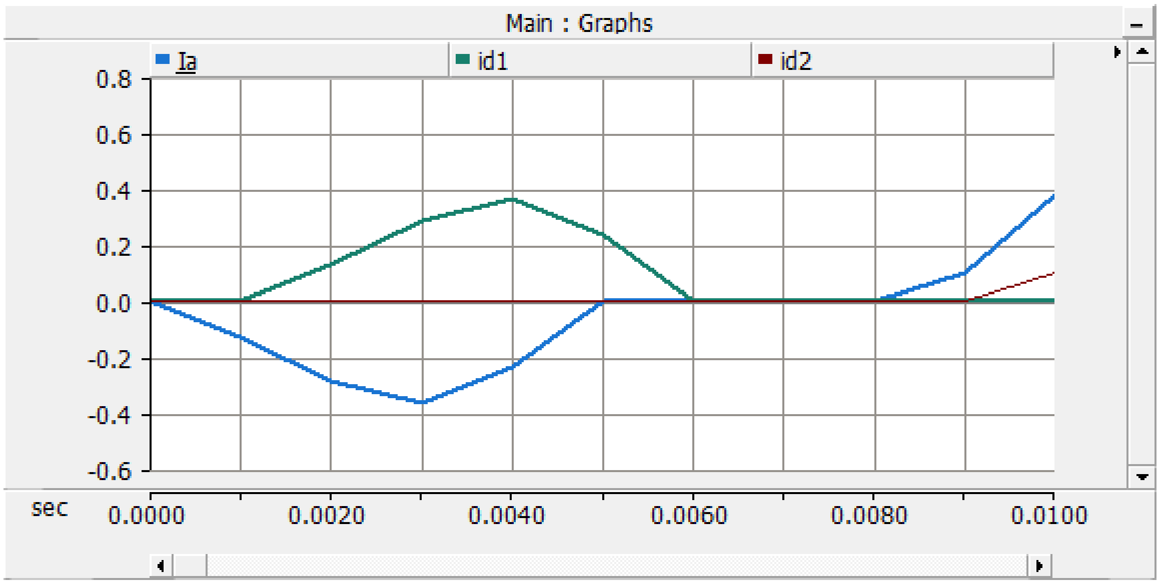

Figure 7: Oscillations of i in a PSCAD simulation of the test circuit using 1 ms time step.

to avoid becoming stuck at $i = 0$. We use the saturation current I_s for the hysteresis. Hence, the transition condition z_u for leaving DU and z_l for leaving DL are

$$z_u(i) = i + I_s \tag{10}$$

$$z_l(i) = i - I_s \tag{11}$$

Fig. 5 shows solutions calculated with this model using several choices for the error tolerance of the corrected Euler algorithm. The root finding algorithm triggers events when their zero crossing functions have passed no more the 10^{-8} beyond the threshold. As before, the maximum step size for the numerical integrator is fixed at 1 ms.

The solutions, shown in Fig. 5, are quite insensitive to the choice of error tolerance, and so is the computational effort. For error tolerance 0.1 we need 1,086 simulation steps, which includes integrator steps and discrete events. For error tolerance 0.01 this is 3,245 steps and events, and for 0.001 we need 9,974 integrator steps and discrete events. Across this range of parameters for the numerical integrator, the solution is free from numerical oscillations of i. The precise transitions to and from $i = 0$ are apparent in Fig. 6.

4 TRAPEZOIDAL METHODS

Our case study uses a single numerical integration method, which differs only in its auxiliary features. That is, the absence or presence of error control for the continuous state variables and an explicit accounting for discrete modes of operation that are entered and exited abruptly as discrete events. Should we change from, say, corrected Euler to the trapezoidal method, the specifics of the simulation results will change. However, the errors caused by omitting discrete modes of operation will remain to cause numerical artifacts.

We illustrate this fact in Fig. 7, which is taken from a simulation of our test circuit using the PSCAD simulator and a 1 ms time step. The current $-i_a$ in this plot is i in our model, and the other currents are through the diodes. PSCAD uses an implicit trapezoidal method with error and stability properties very different from corrected Euler. Event handling in PSCAD is accomplished in three steps (Manitoba Hydro International, Ltd. 2020):

1. interpolating between steps to locate the time of the zero crossing; say at 4.5 ms in our 10 ms simulation;
2. advancing one step from the interpolated solution at 4.5 ms to a new solution at 5.5 ms;
3. back interpolating the state to 5 ms and restarting the simulation.

Numerical artifacts are apparent near the switching moment, which the discrete event simulation places near 4.5 ms. The sum of the currents in Fig. 7 is not equal zero at 5 ms. This is seen again at 1 ms and 9 ms, following the first motion of the voltage source away from zero and the switching on of diode DL, respectively. Interpolation, by assuming a polynomial form of the solution between events, offers no guarantees that the physical constraints described by the model's equations are satisfied. Our discrete event simulator avoids these artifacts by numerically integrating to the moment of the event, applying the discrete changes at that time, and restarting integration from that moment.

5 CONCLUSION

If the presence or absence of an algorithm for precisely handling events visibly alters the simulation results, then why is this not a universal feature of circuit simulators? The answer, almost certainly, is a question of history and economics. Popular circuit simulation tools have their origins in problems of analog electronics, and the trapezoidal method has distinct advantages in this context (Dommel 1986). Moreover, many of these tools have existed for decades and are heavily optimized for their particular domains, in which discrete event dynamics are uncommon.

The introduction of a new simulation method into an existing tool raises several difficult issues. The cost of software changes is obvious. Models built to leverage features of a particular solution method may not work properly if the method of solution is changed. It is also necessary to augment existing models to account for discrete modes of operation, which raises problems of verification and validation.

As we have seen, simulations without event handling can produce usable, if flawed, solutions for models with discrete events. If these flaws have not been resolved, then we may conclude that the cost of doing so is not justified by the perceived increase in useful information (Nutaro and Zeigler 2018). In the context of electric power simulations, it is an open question whether this perception will withhold as power electronics become increasingly important. In anticipation of this emerging future need, our case study sheds light on a numerical problem inherent in widely used tools, identifies its origin, and shows how the problem can be resolved.

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